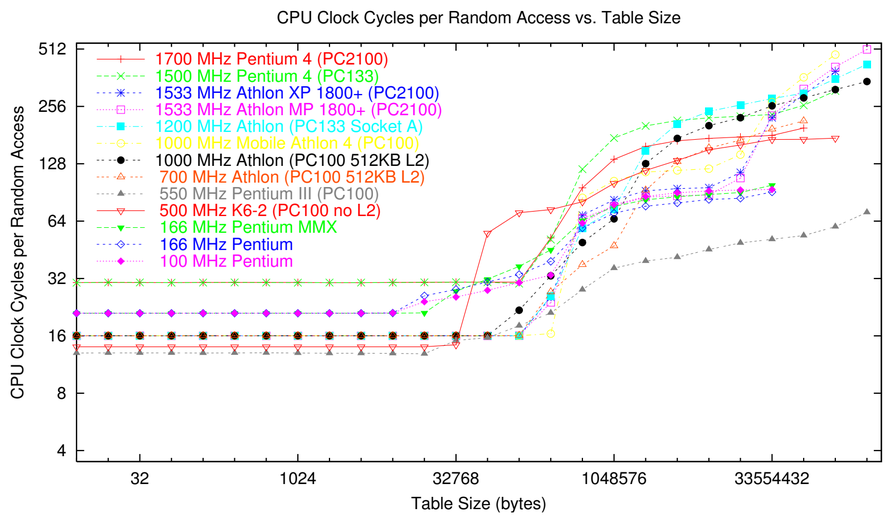
Aggregate.Org

UNBRIDLED COMPUTING

Compilers



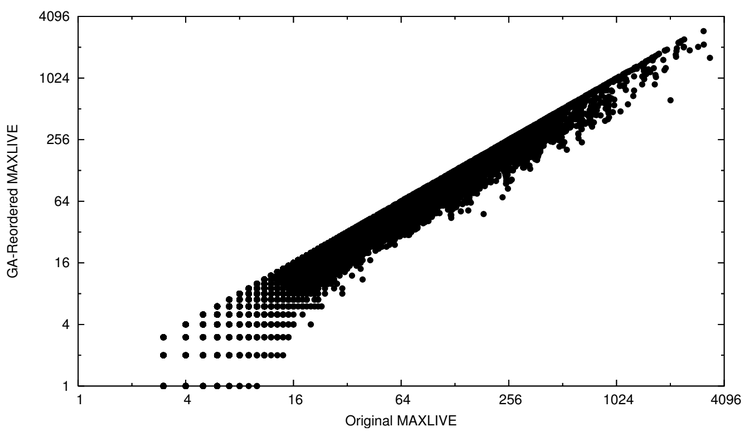
Memory Hierarchy Management:

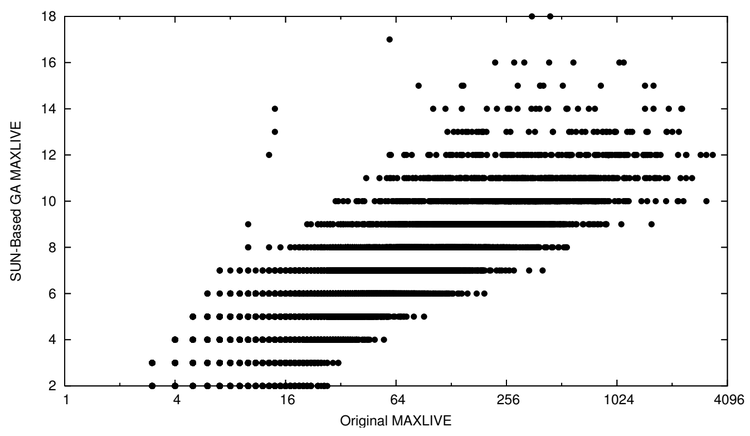
Compressive Hashing...

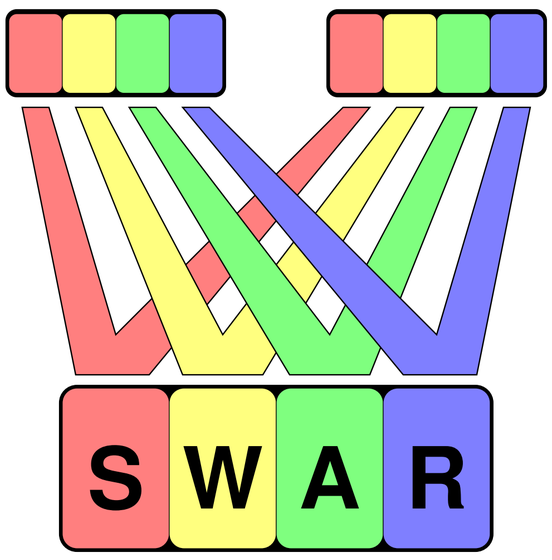
Register/Cache Allocation

Minimize MAXLIVE by

GA Reordering, SUN-GA CSE Reinstantiation







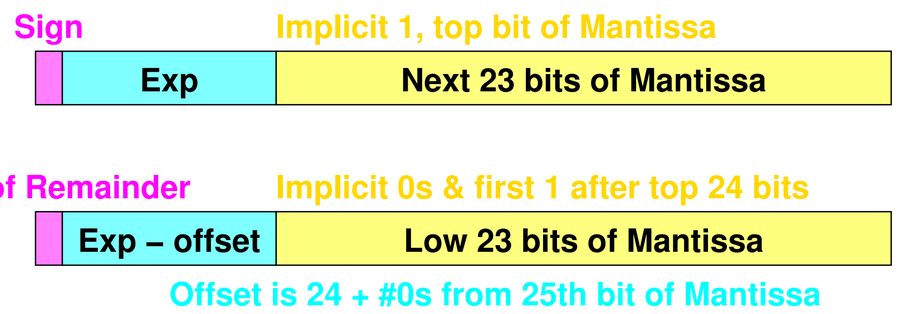
SIMD Within

A Register

GPU/SWAR Native-Pair Floating-Point:

Native 32-bit Float:

Physical layout of Native-Pair Float:

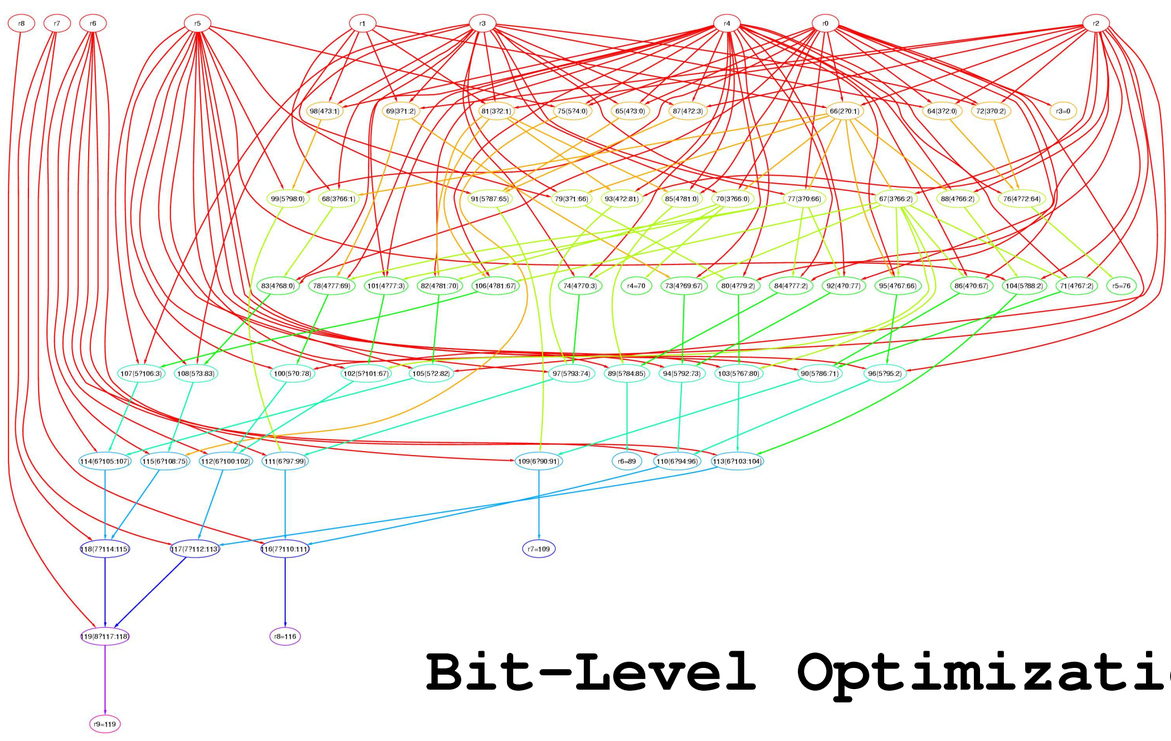


Magic

Algorithms...

PCCTS

Speculative Precision...



Bit-Level Optimization

Meta-State Conversion

(MIMD code, SIMD hardware)