UNIVERSITY OF KENTUCKY College of Engineering

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Line Associative Registers Architecture

Matthew Sparks

Abstract: Modern processor architectures suffer from an ever increasing gap between processor and memory performance. The current memory-register model attempts to hide this gap by a system of cache memory. Several methods of overcoming this gap have been attempted, including cache registers and increasing the number of arithmetic operations performed per memory fetch.

Line Associative Registers, or LARs, are proposed as a new system to avoid the memory gap entirely by pre-fetching and associative updating of both instructions and data. Explictly preloading these LARs with insructions also solves the problem of branch prediction by having both potential branch results available for use. This talk will discuss the concept of a LARs based architecture, and past and current work on LARs within KAOS.

Keywords: memory caching, ambiguous alias, memory gap

Speaker: Matthew Sparks received a BS in Computer Engineering from the University of Kentucky in 2011. His previous work includes internships with North American Stainless and the Department of Defense in machine vision and signal processing. His current research is the development of a line associative register based HDL architecture.

When: Noon to 1PM, Wed., March 21, 2012

Where: 108 Marksbury

RSVP required? no

Refreshments/lunch served? no

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